35 U.S.C. § 102 Rejection —

The Examiner has rejected claims 1-2, 5-7 and 8-9 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,566,174 (Sato). Applicant respectfully traverses this rejection and points out that for cited art to anticipate a claim, that art must disclose each and every limitation of the claim.

Claim 1 recites in pertinent part:

> ... an input packet buffer, ... generating a status signal indicating whether the input packet buffer is: full, empty, or neither empty nor full;
> an output packet stream generator, ... generating the output packet stream in synchronism with the output clock signal,
> a variable output clock signal generator, responsive to a control signal, and
> a control signal generator, responsive to the status signal, and generating the control signal.

Claim 8 recites in pertinent part:

> ... generating a status signal indicating whether the input packet buffer is: full, empty, or neither empty nor full;
> generating the output packet stream in synchronism with the output clock signal;
> generating a variable output clock signal in response to a control signal; and
> generating the control signal in response to the status signal.

By varying the output clock signal in response to the status of the input packet buffer, it is possible to minimize the possibility of input packet buffer underflow or overflow. This is illustrated in Fig. 1 and discussed in detail on page 8, lines 19-25 and page 9, lines 6-11 of the originally filed specification of the present application.

Sato does not disclose a variable output clock signal generator, which varies the output clock signal in response to a control signal, which is generated in response to the status signal from the input packet buffer. In addition, Sato does not disclose an input packet buffer which generates a status signal indicating whether the input packet buffer is: full, empty, or neither empty nor full, as is recited in claims 1 and 8.

Instead, Sato discloses a local clock 39 (Figs. 6 and 7) which produces a fixed output clock signal. There is no illustration of the local clock 39 being variable or receiving a control signal in Figs. 6 or 7, nor any such disclosure in the corresponding portion of the written description. Also, the Examiner has equated buffer 42 in Sato with the input packet buffer recited in claims 1 and 8. However, the status signal produced by buffer 42 of Sato indicates only that there is at least one packet in buffer 42 (col. 9, lines 45-46); i.e. it is either empty or not. There is no disclosure in Sato that buffer 42 produces a status signal indicating whether the input packet buffer is: full, empty, or neither empty nor full, as is recited in claims 1 and 8.

Because Sato does not disclose each and every limitation recited in claims 1 and 8, it cannot anticipate those claims. Claims 2 and 5-7, dependent from and further defining the invention recited in claim 1, and claim 9, dependent from and further defining the invention recited in claim 8, are deemed allowable over Sato for the reasons given above with respect to claims 1 and 8. However, Applicant makes the following specific comments on the indicated claims.

Claim 2 recites in pertinent part:

> ... circuitry to generate the control signal to condition the variable output clock signal generator to increase its frequency if the status signal indicates that the input packet buffer is full, and decrease its frequency if the status signal indicates that the input packet buffer is empty.

Claim 9 recites in pertinent part:

> ... the variable output clock signal increases in frequency if the status signal indicates that the input packet buffer is full, and decreases in frequency if the status signal indicates that the input packet buffer is empty.

Because Sato does not disclose a variable output clock signal generator, and because Sato does not disclose an input packet buffer generating a status signal indicating whether the input packet buffer is full, empty or neither full or empty, as is recited in claims 1 and 8, it cannot include a control signal generator which generates a control signal to condition the variable output clock signal generator to increase its frequency if the status signal indicates that the input packet buffer is full, and decrease its frequency if the status signal indicates that the input packet buffer is empty, as is recited in claims 2 and 9.

For the above reasons, claims 1-2, 5-7 and 8-9 are deemed allowable over Sato. The Examiner is respectfully requested to reconsider and withdraw this rejection.

35 U.S.C. § 103 Rejections —

Applicant states that the subject matter and claimed invention of the present application were, at the time the invention was made, subject to an obligation of assignment to the assignee of the present application.

The Examiner has rejected claims 3 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Sato in view of U.S. Patent 6,169,747 (Sartain). Applicant respectfully traverses this rejection and points out that for a combination of art to render a claim unpatentable, that combination must disclose or suggest each and every limitation of the claim.

Claim 3 is dependent from claim 2 which, in turn, is dependent from independent claim 1. Claim 10 is dependent from claim 9 which, in turn, is dependent from independent claim 8.

Claim 3 recites in pertinent part:

> ... the input packet buffer generates the status signal further indicating whether the input packet buffer is: nearly full, or nearly empty;
>
> the control signal generator further comprises circuitry to generate the control signal to condition the variable output clock signal generator to increase its frequency if the status signal indicates that the input packet buffer is nearly full, and decrease its frequency if the status signal indicates that the input packet buffer is nearly empty.

Claim 10 recites in pertinent part:

> the status signal further indicates whether the input packet buffer is: nearly full, or nearly empty; and
>
> the control signal conditions the variable output clock signal to increase its frequency if the status signal indicates that the input packet buffer is nearly full, and decrease its frequency if the status signal indicates that the input packet buffer is nearly empty.

As discussed in detail above, Sato does not disclose or suggest a variable output clock signal generator nor a control signal generator for controlling the variable output clock signal generator in response to the status of the input packet buffer, nor an input packet buffer generating a status signal to indicate whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claims 1 and 8. Sato further does not disclose or suggest an input packet buffer generating a status signal further indicating whether the input packet buffer is nearly full or nearly empty, as is recited in claims 2 and 9. Because Sato does not disclose or suggest generating a status signal indicating whether the input packet buffer is empty, nearly empty, nearly full, full or neither full nor empty, Sato cannot disclose generating a control signal so that the variable output clock signal generator increases its frequency if the status signal indicates that the input packet buffer is full or nearly full and decreases its frequency if the status signal indicates that the input packet buffer is empty or nearly empty, as is recited in claims 2, 3, 9 and 10.

Sartain also does not disclose a variable output clock signal generator nor a control signal generator for controlling the variable output clock signal generator in response to the status of the input packet buffer, as is recited in claims 1 and 8. Further, Sartain does not disclose generating the control signal so that the variable output clock signal generator increases its frequency if a status signal from an input packet buffer indicates that the input packet buffer is full or nearly full and decreases its frequency if the status signal indicates that the input packet buffer is empty or nearly empty, as is recited in claims 2, 3, 9 and 10.

Instead, Sartain discloses an oversampled DAC system. An input buffer 111 holds input digital samples and generates a status signal indicating underflow, overflow, near underflow and near overflow conditions. Because a DAC system generates an analog signal having a level corresponding to the values of successive input samples, there cannot be a source of an input packet stream, nor an input packet buffer. Also because a DAC system generates an analog output signal, there cannot be an output packet stream generator generating the output packet stream in synchronism with an output clock signal, nor a variable output clock signal generator, nor a control signal generator controlling the output clock signal generator, as is recited in claims 1 and 8.

More specifically, Sartain does disclose a sample input buffer 111 which generates a status signal indicating whether it is full (overflow) or empty (underflow) or nearly full (near overflow) or nearly empty (near underflow). An interpolation filter interpolates a number (e.g. 128 in Sartain) of oversamples in a frame between each input sample received from the input buffer 111. In order to minimize overflow and/or underflow of downstream circuitry, the interpolation filter is controlled in response to the status of the input buffer 111 to vary the number of interpolated oversamples in a frame. In one embodiment (Fig. 6), the coefficients of a variable interpolation filter 145 are varied to change the number of oversamples in a frame (col. 4, lines 28-35). That is, depending on the state of the input buffer 111, either more (e.g. 129) or fewer (e.g. 127) oversamples are produced in a frame (col. 4, lines 60-66). In another

embodiment (Fig. 7), a fixed number (e.g. 128) of oversamples are produced by the interpolation filter 143 but some oversamples are either repeated or dropped (col. 5, lines 12-19). In yet another embodiment (Fig. 8) a fixed number of oversamples (e.g. 128) are produced by the interpolation filter 149, but a master clock 151 is stalled for one or more clock cycles depending on the status of the input buffer 111 (col. 5, lines 62-67). There is no disclosure or suggestion of an output packet stream generator responsive to a variable output clock signal generator whose frequency changes based on the of the input packet buffer being full or nearly full, or empty or nearly empty, as is recited in claims 3 or 10.

Neither of the references cited by the Examiner, taken singly or in combination, disclose or suggest an output packet stream generator responsive to a variable output clock signal generator generating an output clock signal conditioned to increase frequency when the status signal indicates that the input packet buffer is full, or nearly full, and to decrease frequency when the status signal indicates that the input packet buffer is empty or nearly empty, as is recited in claims 3 and 10. Because the combination suggested by the Examiner does not include all of the limitations of claims 3 and 10, that combination cannot be said to render those claims unpatentable. For these reasons claims 3 and 10 are deemed allowable over Sato and Sartain and the Examiner is respectfully requested to reconsider and withdraw this rejection.

The Examiner also rejected claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Sato. Applicant respectfully traverses this rejection and points out that for a reference to support a 35 U.S.C. § 103(a) rejection, that reference must provide a motivation to be modified in the manner suggested by the Examiner.

Claim 4 recites in pertinent part, "... if the status signal indicates that the input packet buffer is full, null packets are deleted from the input transport packet buffer."

As discussed in detail above, Sato does not disclose or suggest a variable output clock signal generator nor a control signal generator for controlling the variable output clock signal

generator in response to the status of the input packet buffer, nor an input packet buffer generating a status signal to indicate whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 1. Sato also does not disclose or suggest deleting null packets from the input transport packet buffer if the status signal indicates that the input packet buffer is full, as is recited in claim 4.

Instead, referring to Fig. 3 of Sato, Sato discloses circuitry 82 for unconditionally removing any null packet from the input packet stream (col. 5, lines 30-31). Furthermore, the buffer 42, specified by the Examiner as corresponding to the input packet buffer recited in claim 1, does not provide a status signal indicating that it is full. Instead, the status signal from buffer 42 indicates only that there is at least one packet in the buffer 42, i.e. whether the buffer is empty or not (col. 9, lines 45-46). Because Sato already discloses circuitry for handling null packets in the input packet stream, there is no motivation to modify Sato in the extensive manner suggested by the Examiner to handle null packets in a the manner recited in claim 4.

Applicant, therefore, respectfully suggests that there is nothing in Sato which would lead one skilled in the art to make the modifications suggested by the Examiner. Instead, the Examiner was led to suggest his modifications to Sato only because of Applicant's own disclosure. This is impermissible hindsight. Further, as described above, Sato does not disclose or suggest a variable output clock signal generator nor a control signal generator for controlling the variable output clock signal generator in response to the status of the input packet buffer, nor an input packet buffer generating a status signal to indicate whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 1. Sato also does not disclose or suggest deleting null packets from the input transport packet buffer if the status signal indicates that the input packet buffer is full, as is recited in claim 4. Sato, therefore, does not disclose or suggest each and every limitation of claim 4. For these reasons, Applicant deems claim 4 allowable over Sato and respectfully requests the Examiner to reconsider and withdraw this rejection.

The Examiner has also rejected claim 12 under 35 U.S.C. § 103(a) as being unpatentable over Sato in view of U.S. Patent 5,969,770 (Horton). Applicant respectfully traverses this rejection.

Claim 12 is dependent from independent claim 8. Claim 12 recites in pertinent part, "... the source of input transport packet stream represents auxiliary on-screen display (OSD) information."

As discussed in detail above, Sato does not disclose or suggest a generating a variable output clock signal responsive to a control signal, nor generating a control signal in response to the status signal from an input packet buffer, nor generating an input packet buffer status signal indicating whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 8. Referring to Fig. 3, while Sato does disclose a source 16 of auxiliary packets to be multiplexed into the packet stream to be recorded, that auxiliary packet source does not carry data representing on-screen display information, as is recited in claim 12. Instead, these auxiliary packets are termed "trickmode" packets in Sato. There is no detailed description in Sato of what trickmode packets are, but it is stated that trickmode packets "can be generated from the incoming transport stream." This does not suggest the use of trickmode packets for on-screen display information, which are generally independent of the incoming transport packet stream and usually predetermined fixed images which are stored in a read-only memory (ROM).

Horton does not disclose or suggest generating an output packet stream in synchronism with the output clock signal, as is recited in claim 8. Because Horton does not disclose or suggest generating an output packet stream, it cannot disclose or suggest generating a variable output clock signal in response to a control signal, nor generating a control signal in response to the status of the input packet buffer, nor generating a status signal to indicate whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 8.

Instead, Horton discloses a receiver for receiving a transport packet stream (1507) and processing the packet stream to produce the sound (21a, 21b) and image (19) of the selected television program, including selected on-screen display images produced from MPEG graphics information (1525-5) previously stored in the ROM 1525. Input packets are received and stored in an input packet buffer 1513, the data in the packets is then extracted and used to produce the sound and image of the television program. MPEG packets representing an on-screen display are stored in ROM 1525 and are processed in the transport processor 1507, as appropriate, to generate the on-screen display. There is no output packet stream.

Neither Sato nor Horton disclose or suggest generating a variable output clock signal nor generating a control signal for controlling the variable output clock signal in response to the status of the input packet buffer, nor generating a status signal to indicate whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 8. Because the combination of Sato and Horton suggested by the Examiner does not disclose or suggest every limitation of claim 12 (dependent from claim 8), it cannot be said to render claim 12 unpatentable. For this reason claim 12 is deemed allowable over Sato and Horton. The Examiner is respectfully requested to reconsider and withdraw this rejection.

The Examiner has also rejected claims 11 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Sato in view of U.S. Patent 5,734,589 (Kostreski). Applicant respectfully traverses this rejection.

Claim 11 is dependent from independent claim 8, and recites in pertinent part, "... the input packet stream format is compatible with one of a QAM or QPSK modulation format; and the output packet stream format is compatible with an 8-VSB or 16-VSB modulation format."

Claim 13 is dependent from independent claim 8, and recites in pertinent part, "... the input packet stream format is compatible with one of QAM, QPSK or VSB modulation formats;

and the output packet stream format is compatible with a different one of said QAM, QPSK or VSB modulation formats."

As discussed in detail above, Sato does not disclose or suggest a generating a variable output clock signal responsive to a control signal, nor generating a control signal in response to the status signal from an input packet buffer, nor generating an input packet buffer status signal indicating whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 8.

Kostreski also does not disclose or suggest generating a status signal indicating whether an input packet buffer is full, empty or neither empty nor full, nor generating a variable output clock signal in response to a control signal, nor generating the control signal in response to the status signal, as is recited in claim 8.

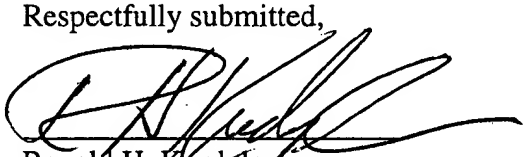
Instead, Kostreski discloses a television and digital signal (audio, video, data) distribution system. The essence of Kostreski is that set top boxes at consumer locations include a processor which can receive programs and data dynamically via one or more channels transmitted through the distribution system. Referring to Fig. 3, analog television signals are received in analog AM-VSB form (316), digital television signals are received in MPEG format (318), and other digital signals are received in ATM packets (401), possibly modulated in any one of several disclosed formats: QPSK, QAM, VSB, etc. The television and digital signals are converted to RF channels and combined (315), and then supplied (303) to a distribution network (309,311) in any one of several disclosed formats, which may be different from the format in which the data was received. While the presence of input packet buffers in the system of Kostreski may be implied by the illustrated packet processing, there is no disclosure of any method for controlling the timing of the processing of those packets, and in particular no disclosure or suggestion of generating a variable output clock signal. More specifically, there is no disclosure or suggestion of generating a variable output clock signal responsive to a control signal, nor generating a control signal in response to the status signal from an input packet buffer, nor generating an input

packet buffer status signal indicating whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 8.

Because neither Sato nor Kostreski disclose or suggest generating a status signal indicating whether an input packet buffer is full, empty or neither empty nor full, nor generating a variable output clock signal in response to a control signal, nor generating the control signal in response to the status signal, as is recited in claim 8, the combination of these references suggested by the Examiner does not disclose or suggest each and every limitation of claims 11 and 13. Therefore, they cannot be said to render claims 11 or 13, dependent from claim 8, unpatentable. Claims 11 and 13, therefore, are deemed allowable, and the Examiner is respectfully requested to reconsider and withdraw this rejection.

In view of the above amendments and arguments, claims 1-13 are deemed allowable. The Examiner is respectfully requested to reconsider and withdraw the rejections, and to allow the application.

Respectfully submitted,



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